


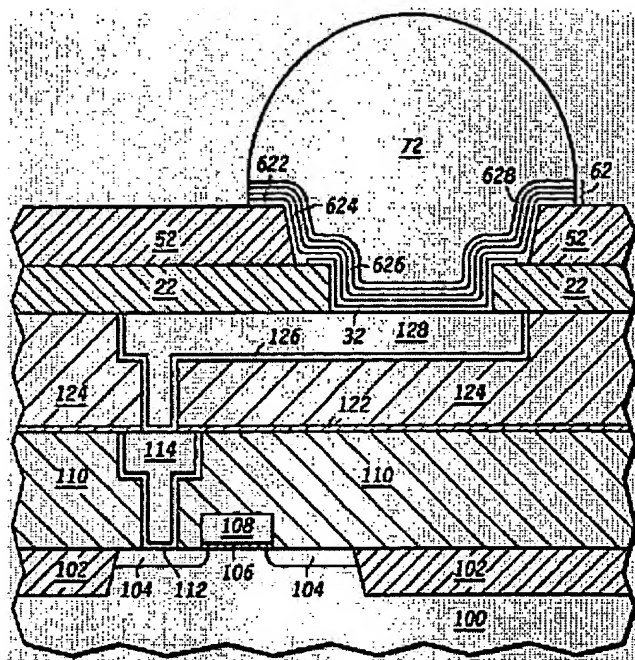


BEST AVAILABLE COPY**Semiconductor device and producing method thereof****Patent number:** CN1269607**Publication date:** 2000-10-11**Inventor:** BAR ALXANDA L (US); VANCARTSAN SULERSH (US);
CLERGE DAVID B (US)**Applicant:** MOTOROLA CO (US)**Classification:****- International:** *H01L21/60; H01L21/768; H01L23/485; H01L23/532;
H01L21/02; H01L21/70; H01L23/48; H01L23/52; (IPC1-
7): H01L23/522; H01L21/28; H01L21/768***- european:** *H01L21/60B2; H01L21/768B; H01L21/768B2D;
H01L21/768C3; H01L21/768C4; H01L23/485B;
H01L23/532M1C2; H01L23/532M1C4***Application number:** CN20000104927 20000404**Priority number(s):** US19990285666 19990405**Also published as:** US2002000665 (A1)
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Abstract not available for CN1269607

Abstract of correspondent: **US2002000665**

An interconnect overlies a semiconductor device substrate (10). In one embodiment, a conductive barrier layer overlies a portion of the interconnect, a passivation layer (92) overlies the conductive barrier layer and the passivation layer (92) has an opening that exposes portions of the conductive barrier layer (82). In an alternate embodiment a passivation layer (22) overlies the interconnect, the passivation layer (22) has an opening (24) that exposes the interconnect and a conductive barrier layer (32) overlies the interconnect within the opening (24).



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